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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,553	03/25/2004	Charles Ray Johns	AUS920030696US1	7923

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IBM CORP. (WIP)
c/o WALDER INTELLECTUAL PROPERTY LAW, P.C.
P.O. BOX 832745
RICHARDSON, TX 75083

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,553	JOHNS ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 12/27/2006 have been fully considered but they are not persuasive. Rejection of claim 6 under 35 U.S.C. 112 first paragraph is withdrawn. Currently, claims 1-21 are pending for examination.

2. In responding to applicant's arguments regarding independent claims 1, 9 and 15 rejected under 35 U.S.C. 102(e) that Futral fail to teach or suggest the claimed limitation "DMA controller that is configured to execute DMA commands for management of a cache," because the word "cache" does not appear anywhere in the Futral reference, as stated on page 7, 1st paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

In accordance to the applicant's remarks, on page 8, last paragraph, "a cache is a storage that keeps frequently accessed data or program instruction readily available so that the device, in this case a DMA controller, does not access then repeatedly from slower storage.

As cited by the examiner from the preceding office action, in paragraph [0015] from Futral, "...the DMA controller 122 may process a DMA command structure 124 and perform data transfers that involve buffer 126 and/or I/O device 120 per the DMA command structure 124...". Furthermore, only for the purpose of clarifying the terminology, the definition of "direct memory access (DMA)" in accordance to the

"Microsoft Computer Dictionary" states "memory access that does not involve the microprocessor and is frequently used for data transfer directly between memory and an "intelligent" peripheral device." Therefore, the DMA controller (Fig. 1, ref. 122) will process the DMA command structure (i.e. DMA commands) (Fig. 1, ref. 124) and perform frequent data transfers that involve the memory's (Fig. 1, ref. 116) buffer (Fig. 1, ref. 126) and/or I/O device (Fig. 1, ref. 120).

In conclusion, Futral does teach the claimed limitation "DMA controller that is configured to execute DMA commands for management of a cache," wherein Futral's memory (Fig. 1, ref. 116) is the cache that is accessed by the DMA controller (Fig. 1, ref. 122) for cache management comprising frequent DMA data transferring.

3. In responding to applicant's arguments regarding the dependent claims 2, 7, 8, 10, 13, 14, 20, and 21 rejected under 35 U.S.C. 103(a) that neither Futral nor Olivier teach or suggest the claimed "a cache" or "DMA controller that is configured to execute DMA commands for management of a cache," as stated on page 9, 2nd paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Please view the examiner's detail response, as discussed above, regarding that the claimed limitations "a cache" or "DMA controller that is configured to execute DMA commands for management of a cache" are disclosed by Futral.

4. In responding to applicant's argument regarding the dependent claims 4, 5, 12, 18 and 19 rejected under 35 U.S.C. 103(a) that the combined references of Futral and

Liao does not teach or suggest every claimed limitation because neither Futral nor Liao teach or suggest providing DMA commands for cache management or a DMA controller that is configured to execute DMA commands for management of a cache, as stated on page 10, 1st paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Please view the examiner's detail response, as discussed above, regarding that the claimed limitations "DMA controller that is configured to execute DMA commands for management of a cache" are disclosed by Futral. Furthermore, the DMA commands would reside in Futral's DMA command structure (Futral, Fig. 1, ref. 124).

5. In responding to all applicant's arguments, the examiner will maintain his position and the current rejection of record.

i. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

6. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

7. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

8. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated September 28, 2006 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 3, 9, 11, 15 and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Futral et al. (US Pub.: 2005/0033874).

10. As per claims 1, 9 and 15, Futral teaches a system, a method, and a computer program product having a medium with a computer program embodied thereon to provide software program control of cache management, comprising:

a processor (Fig. 1, ref. 102) and a DMA controller (Fig. 1, ref. 122);

the processor configured to generate DMA commands for the management of a cache (Fig. 1, ref. 116) on the execution of a software program on the processor

([0001], [0011] and [0015]), wherein the processor commands by requesting the DMA controller to transfer data to/from the cache; and

the DMA controller coupled to the processor, configured to execute the DMA commands for the management of a cache ([0001], [0011] and [0015]), wherein the DMA controller implement the transferring of data in accordance to the request from the processor.

11. As per claims 3, 11 and 16-17, Futral teaches the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising:

wherein at least one of the DMA commands is a get command (e.g. to read data from the cache) ([0021]) and

at least one of the DMA commands is a put command (e.g. to store data into the cache) ([0022]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2, 7-8, 10, 13-14 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Futral et al. (US Pub.: 2005/0033874) in view of Ollivier et al. (US Patent 6,738,881).

Futral teaches all the limitations of claims 1, 9 and 15 as discussed above, where Futral teaches the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising wherein the memory (Fig. 1, ref. 116) is coupled to the DMA controller (Fig. 1, ref. 122)

Futral does not teaches the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising:

a cache coupled to the DMA controller, the system configured for the execution of the DMA commands for the management of a cache on the DMA controller to manage the operation of the cache coupled to the DMA controller;

wherein the cache is a DMA cache tightly coupled to the DMA controller; and

wherein the cache is a cache for system memory.

Ollivier teaches a system and a method comprising:

implementing a DMA data transferring to and from a plurality of memories (Fig. 2, ref. 220, 222, 224) by utilizing a DMA controller (Fig. 2, ref. 210), wherein the plurality of memories are coupled to the DMA controller and are memories of the system (Fig. 2, ref. 100) (col. 3, l. 57 to col. 4, l. 3); and

the DMA controller further include a plurality of FIFOs (Fig. 3A, ref. FIFO 0, FIFO 1, FIFO 2, FIFO 3, FIFO 4, FIFO 5), wherein the plurality of FIFOs are utilized to manage the data transferring to and from the plurality of memories (Fig. 2, ref. 220, 222, 224) (col. 3, l. 57 to col. 4, l. 3 and col. 5, ll. 39-50).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Ollivier's plurality of memories and plurality of FIFOs into Futral's system of cache management. The resulting combination of the references further teaches the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising:

the plurality of memory coupled to the DMA controller, wherein the DMA command is executed for transferring data to and from the plurality of FIFOs on the DMA controller, in order to transfer data to and from the plurality of memories coupled to the DMA controller

wherein the plurality of FIFOs (i.e. DMA cache) are tightly coupled to the DMA controller; and

wherein the plurality of memories are the cache for system.

Therefore, it would have been obvious to combine Ollivier with Futral for the benefit of improving the performance of a processor (Ollivier, col. 1, ll. 48-51).

13. Claims 4-5, 12 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Futral et al. (US Pub.: 2005/0033874) in view of Liao et al. (US Patent 6,681,296).

Futral teaches all the limitations of claims 1, 9 and 15 as discussed above.

Futral does not expressly teach the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising:

wherein at least one of the DMA commands is a flush command and

wherein at least one of the DMA commands is a zero command.

Liao teaches a cache management system and method comprising:

a "block flush" command (col. 3, ll. 8-23); and

a "block set to zero" command (i.e. zero command) (col. 3, ll. 8-23).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Liao's "block flush" and "block set to zero" commands into Futral's system of cache management.

Therefore, it would have been obvious to combine Liao with Futral for the benefit of more efficient utilization of on-chip cache (Liao, col. 4, ll. 47-53).

14. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Futral et al. (US Pub.: 2005/0033874) in view of Ohba (US Patent 6,427,201).

Futral teaches all the limitations of claim 1 as discussed above, where Futral teaches the system to provide software program control of cache management,

comprising wherein the parameters of the DMA commands comprise a transfer size (size 204 of Fig. 2) and a source (Fig. 2, ref. 200) comprises the physical address for the start location (Fig. 2, ref. 210), wherein the size is utilized in defining the physical address for the end location (i.e. effective address low) ([0017] and [0021]), as the effective address is defied by the start location and the end location.

Futral does not expressly teach the system to provide software program control of cache management, comprising wherein the parameters of the DMA commands comprise tag.

Ohba teaches a system and a method comprising a DMA packet including a tag-command (DMA-tag) (Fig. 6 and col. 7, l. 64 to col. 8, l. 3).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Ohba's tag-command into Futral's DMA commands. The resulting combination of the references further teaches the system to provide software program control of cache management, comprising wherein the parameters of the DMA commands comprise tag-command, size and end location of the physical address.

Therefore, it would have been obvious to combine Ohba with Futral for the benefit of providing an information processing device for efficiently performing various processing operations (Ohba, col. 1, ll. 58-63).

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-21 have received a final action on the merits. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

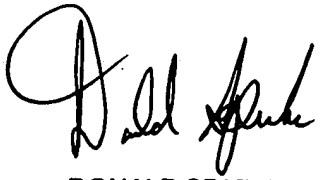
IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 09, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181



DONALD SPARKS
SUPERVISORY PATENT EXAMINER